

# Persistence and Synchronization: Friends or Foes?

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**Abstract**—Emerging non-volatile memory (NVM) technologies promise memory speed byte-addressable persistent storage with a load/store interface. However, programming applications to directly manipulate NVM data is complex and error-prone. Applications generally employ libraries that hide the low-level details of the hardware and provide a transactional programming model to achieve crash-consistency. Furthermore, applications continue to expect correctness during concurrent executions, achieved through the use of synchronization. To achieve this, applications seek well-known ACID guarantees. However, realizing this presents designers of transactional systems with a range of choices in how to combine several low-level techniques, given target hardware features and workload characteristics.

In this paper, we provide a comprehensive evaluation of the impact of combining existing crash-consistency and synchronization methods for achieving performant and correct NVM transactional systems. We consider different hardware characteristics, in terms of support for hardware transactional memory (HTM) and the boundaries of the persistence domain (transient or persistent caches). By characterizing persistent transactional systems in terms of their properties, we make it possible to better understand the tradeoffs of different implementations and to arrive at better design choices for providing ACID guarantees. We use both real hardware with Intel Optane DC persistent memory and simulation to evaluate a persistent version of hardware transactional memory, a persistent version of software transactional memory, and undo/redo logging. Through our empirical study, we show two major factors that impact the cost of supporting persistence in transactional systems: the persistence domain (transient or persistent caches) and application characteristics, such as transaction size and parallelism.

## I. INTRODUCTION

Emerging Non-Volatile Memory (NVM) technologies, like Intel’s 3D XPoint [1], offer byte-addressability and orders of magnitude faster access to storage than traditional storage technologies. Their key appeal is that they allow applications to access storage directly using processor load and store instructions rather than relying on a software intermediary like the file system or a database [2]. However, ensuring that data stored in NVM is always in a safe and recoverable state is both hard and incurs performance overheads [2]–[5].

To ensure data recoverability, application developers have to carefully orchestrate data movement from the volatile to the persistent components in the memory hierarchy, subject to application-specific constraints. This task is especially complex due to two factors: (1) NVM applications have very diverse crash-consistency requirements [6]; and (2) the *persistence domain* is different across platforms. For example, Intel and Micron guarantee that data becomes persistent only when it reaches the memory controller of the NVM device, i.e., the persistence domain of the system includes the memory controller and the NVM devices [7]. We refer to such systems as having *transient caches*. However, HPE’s NVM [8] guarantees that the entire cache hierarchy is persistent, i.e., the persistence domain includes the entire memory hierarchy. We refer to such systems as having *persistent caches*.

In this context, researchers have proposed various transactional systems that provide the well known “ACID” guarantees for NVM applications [4], [5], [9]–[13]. These transactional systems significantly simplify NVM application development and leave the complexities of achieving data recoverability on various platforms to the low-level systems software developers. While these systems all provide ACID

guarantees, they go about providing these guarantees in different ways: UNDO vs. REDO logging, software vs. hardware transactions. Low-level developers designing ACID transaction systems face a bewildering array of choices, with varied performance characteristics that change with the applications and the platform used. For these developers, we aim to answer the question: **how to quickly explore the design space and arrive at a correct and high-performance implementation of a NVM transactional system?**

Reasoning about implementation details rather than the overall guarantees provided to the user (ACID) helps transaction system developers traverse the design-space more efficiently. To provide ACID guarantees, the underlying transaction system has to correctly ensure three properties: (1) *crash consistency* - individual transactions are failure-atomic, i.e., after a crash, either all or none of the transaction has persisted, (2) *synchronization* - transactions are correctly isolated from other transactions executed on different threads, and (3) *composability* - the crash consistency and synchronization techniques used compose to provide the overall ACID guarantees, by ensuring that dependent transactions are correctly ordered.

This new characterization of transaction systems provides a basis to compare different implementations and to identify the right set of *crash-consistency* and *synchronization* mechanisms for particular applications and hardware platforms. We perform a detailed characterization study of systems with different implementations (hardware transactional memory (HTM) [12], software transactional memory (STM) [4], and *undo/redo* logging with locks [4], [14]) under various persistence domains (transient vs. persistent caches). We perform our study on real hardware using the recently released Intel’s DC Optane Persistent Memory [15] and using simulation.

Our empirical study results in several interesting insights for NVM transaction system developers:

- 1) For all applications, the persistence domain plays the most important role. The overhead of making transactions persistent is considerably lower when caches are persistent.
- 2) In systems with transient caches, HTM is the best choice, despite its synchronization costs and required architectural changes. This is due to the high overheads caused by flush and fence instructions required by *undo/redo* logs, which are elided by HTM. The choice between *undo* and *redo* logs depends on the application characteristics and the size of the read and write sets of the transactions.
- 3) In systems with persistent caches, the HTM does not require any architectural changes, but its benefit for supporting persistent transactions is reduced, as software logging mechanisms do not require expensive flush and fence instructions anymore. Here, *undo* logs are the best choice because *redo* logs suffer from read-indirection overheads.
- 4) The overheads of crash-consistency for an HTM are subsumed by synchronization overheads. As applications scale, performance increases despite crash-consistency overheads. When the crash-consistent HTM does not achieve scalability due to aborts, crash-consistent STM ensures this property.

Overall, this paper makes the following contributions:

	Baseline Tx	Undo Tx	Redo Tx
1	tx_begin();	tx_begin();	tx_begin();
2	pA = x;	log[&pA] = pA; clwb(log[&pA]); sfence; pA = x;	log[pA] = x;
3	y = pA;	y = pA;	y = (log[pA]    pA);
4	pB = z;	log[&pB] = pB; clwb(log[&pB]); sfence; pB = z;	log[pB] = z;
5	tx_end();	persist_write-set(); commit_log();	clwb(log[pA]); clwb(log[pB]); sfence; commit_log();
6		tx_end();	replay_log(); persist_write-set();
7			tx_end();

TABLE I

UNDO VS REDO LOGGING; UNDO LOGGING SUFFERS FROM FREQUENT CACHELINE FLUSHES AND SFENCES WHILE REDO LOGGING SUFFERS FROM READ-INDIRECTION OVERHEADS.

- We characterize persistent transactions to quickly and methodically compare different implementations of NVM transactional systems that provide ACID guarantees.
- Using this new characterization, we study the performance of various transaction system implementations on different hardware platforms and for different applications.
- We show that there is no one best way to provide ACID guarantees for NVM applications; the best way changes with hardware platforms and application characteristics.
- Finally, we believe we are the first work to evaluate these different transactional systems on real 3D XPoint devices.

## II. BACKGROUND

In order to illustrate the complexity of the design space, we briefly survey different implementations for crash-consistency (§II-A), for transaction synchronization (§II-B), and the impact of the hardware persistence domain on the relationship between the two (§II-C).

### A. Crash-consistent transactions

Crash-consistent (failure-atomic) transactions ensure that a group of updates to NVM locations performed by an application persist atomically, i.e., either all of them are observable or none of them are observable after a failure. Transactions are specified using `tx_begin()` and `tx_end()` calls. All the updates to NVM between those two successive calls are guaranteed to persist atomically. For example, in Table II, the updates to pA and pB are crash-consistent. *Crash-consistency* is generally achieved using undo or redo logging.

**undo logging** is a crash consistency technique that provides failure atomicity by undo-ing (or rolling back) changes from an aborted failure-atomic transaction. To be able to roll back changes, undo logging systems create an undo log entry *prior* to every update performed within the transaction. The undo log entry contains the current value of the memory location/variable that is being updated. Once the log entry had been created and persisted, only then is the actual memory location/variable updated. If a transaction succeeds, all the memory locations modified within the transaction are persisted and then a commit message is atomically persisted to the log to invalidate the log entries belonging to the transaction. If a transaction fails, during the recovery process, all valid log entries are used to roll back partial changes from a transaction. Table I illustrates the operations which need to be performed when using different logging techniques. While certain optimizations may be applicable under some scenarios, the code snippets represent the steps necessary in the general case. As shown in the table, undo logging systems must ensure that: (1) within a transaction, log entries must be created and persisted prior to every update and (2) at the end of the transaction, all memory locations modified within the transaction must be persisted before transaction commit.

**redo logging** is a crash-consistency technique that provides failure atomicity by redo-ing (or rolling forward) changes from committed failure-atomic transactions. To be able to roll forward changes, redo logging systems create a redo log entry for every update within the transaction. The redo log entries contain the latest updates while the actual data is maintained at a prior crash-consistent state. All the read requests for the memory locations updated within the transaction are serviced from the redo log. If a transaction succeeds, a commit log entry is created and persisted in the redo log, marking the commit of the transaction. In the event of a failure, the redo log entries of committed transactions are used to roll forward the application's data to its most recent crash consistent state. The log entries of uncommitted transactions are simply discarded. Periodically, the redo log can be truncated to reduce read indirections and to reduce the number of redo log entries that have to be applied during recovery. As shown in Table I, redo logging systems must ensure that: (1) within a transaction, a redo log entry must be created for every update within the transaction and read requests to these locations must be re-directed to the log, and (2) at the end of the transaction, all the redo log entries and a commit log entry must be persisted.

### B. Transactional memory

Transactional memory [16], [17] is used to synchronize the access of multiple threads to shared program data. Programmers enclose the critical code blocks with `tx_begin()` and `tx_end()` calls. Transactional memory guarantees the atomic execution of a transaction, using speculation. If the runtime detects a conflict with another transaction, it aborts one of the transactions, discards its speculative state and rolls back its execution to the `tx_begin()` call. Software transactional memory (STM) [18] is implemented using fine grained locking and write set logging in software. Hardware transactional memory (HTM) [16] is implemented using the L1 cache to buffer speculative writes and the cache-coherency protocol to detect conflicts with other threads. Current HTM implementations, such as Intel Transactional Synchronization Extensions (TSX), are best effort – transactions could abort for any reason, such as exceeding the L1 cache capacity, using unsupported instructions, or due to interrupts. Therefore, HTMs require a fallback mechanism to ensure progress, usually implemented using locking.

THREAD-1	THREAD-2
tx_begin();	tx_begin();
pA = x;	if (pA == x)
pB = y;	pD = z;
tx_end();	pC = w;
	tx_end();

TABLE II

THREADS EXECUTING DEPENDENT TRANSACTIONS. CORRECT IMPLEMENTATIONS ENSURE THAT pA PERSISTS BEFORE pD, CRASH CONSISTENCY MIGHT BE VIOLATED OTHERWISE.

### C. Persistent and transient caches

There is much diversity among the types of NVM technologies that are available on the market, as different vendors provide different performance characteristics and persistence guarantees. For example, HPE offers a battery-backed DRAM solution [19]. As this design is based on DRAM, the exposed NVM’s latency and bandwidth are as good as for DRAM. In addition, the battery can extend the persistency domain to the entire memory hierarchy, including CPU caches. **Persistent caches** ensure that all modified cache lines are effectively persistent. On the other hand, Intel and Micron’s proposed 3D XPoint technology [1] has higher latency and lower bandwidth than DRAM, while the persistent domain includes only the memory controller, but not the CPU caches [7]. In case of a power failure, **transient caches** will lose modified data not already written back to the memory controller. So, the transaction system developer must use the appropriate instruction sequences to ensure that data becomes persistent on different hardware platforms.

### III. CRASH-SYNC-SAFETY

In this work, we focus on applications that use a transactional programming model to get ACID guarantees. For example, in Table II, updates within each transaction need to provide all or nothing semantics when the data gets to NVM. Providing ACID guarantees requires that the transactional system correctly implement three components: (1) *crash-consistency* (also called failure-atomicity), which ensures all-or-nothing behavior of uncommitted transactions when a failure happens and the validity of the data after the failure (atomicity and consistency) (2) *synchronization*, which ensures that partial updates are not observable by other concurrently running transactions (isolation), and (3) *persistence* of the committed transactions in the correct order, which ensures that committed transaction are made durable and that the correct dependencies between transactions are maintained (durability). Note that crash-consistency is a property of uncommitted transactions, which guarantees that on a failure, a transaction will either abort, leaving no side-effects, or will commit, finishing its entire execution. In contrast, persistence is a property of committed transactions, guaranteeing their permanence in case of a crash, as well as that dependent transactions’ effects are all visible in the correct order. We call a correct implementation of the above three properties that ensures ACID guarantees *crash-sync-safe*.

Programmers identify regions of code within their applications as transactions using `tx_begin()` and `tx_end()`, and are assured of the failure-atomicity of the updates within any transaction. Furthermore, all the updates within the transaction become atomically visible to any other thread in the system once persisted, and conflicting transactions (transactions accessing common memory locations with at least one of the accesses being a write) execute in isolation. So, each transaction behaves as both a traditional transactional memory transaction and also a failure-atomic transaction.

Developers have a wide variety of choices for *crash-sync-safe* transactions, and choosing between these different options depends on a variety of factors, such as the persistence domain, and the application characteristics. To further complicate matters, some mechanisms offer some of the guarantees, but not all, and developers need to carefully mix and match techniques to ensure correctness. For example, `undo` and `redo` logging can be used to implement crash-consistent transactions for single-thread applications, but do not ensure the correct synchronization of multi-threaded applications, forgoing isolation. Conversely, locking can be used to provide correct synchronization for multi-threaded applications, but cannot ensure persistence for these transactions in

	ST – CC		MT – Sync.	MT – CSS	
	TC	PC		TC	PC
seq	✗	✗	✗	✗	✗
HTM+seq (+spinlock)	✗	✗	✓	✗	✗
undo/redo (+spinlock)	✓	✓	✓	✓	✓
HTM+undo/redo (+spinlock)	approx.	✓	✓	approx.	✓
ccHTM+undo/redo (+spinlock)	✓	N/A	✓	✓	N/A
STM	✗	✓	✓	✗	✓
ccSTM	✓	N/A	✓	✓	N/A

TABLE III

CRASH-CONSISTENCY AND CRASH-SYNC-SAFETY IMPLEMENTATIONS FOR SINGLE- AND MULTI-THREADED APPLICATIONS. ST: SINGLE-THREADED, MT: MULTI-THREADED, CC: CRASH-CONSISTENT, SYNC: SYNCHRONIZATION, CSS: CRASH-SYNC-SAFETY, TC: TRANSIENT CACHES AND PT: PERSISTENT CACHES. TECHNIQUES EVALUATED FOR SINGLE-THREADED APPLICATIONS NEED TO PROVIDE ONLY CRASH CONSISTENCY. TECHNIQUES EVALUATED FOR MULTI-THREADED APPLICATIONS PROVIDE SYNCHRONIZATION TOO, BY USING A SPINLOCK WHERE NECESSARY. WE NOTE THAT THE HTM+UNDO/REDO IMPLEMENTATIONS FOR TRANSIENT CACHES ARE ONLY APPROXIMATING A CRASH-SYNC-SAFE SOLUTION.

case of a failure, forgoing durability, nor crash-consistency, forgoing atomicity and consistency. Transactional memory provides correct synchronization for multi-threaded applications, as well as atomicity and consistency, but cannot ensure persistence for these transactions in case of a failure, forgoing durability.

### IV. CRASH-SYNC-SAFE TRANSACTIONS

This section describes different implementations of a transactional library that ensures *crash-sync-safe* in detail. First, to achieve proper synchronization, transactions may be implemented using one of three broad approaches: (1) Hardware Transactional Memory (HTM), (2) Software Transactional Memory (STM), or (3) global locking. Each of these approaches can further be extended to additionally provide *crash-sync-safe* for transactions. Depending on whether the system has transient or persistent caches, the implementation details will vary. Next, we describe these different implementations (Table III).

#### A. Crash-sync-safe HTM

Hardware Transactional Memory (HTM) offers atomicity and isolated transactions for volatile memory. With persistent memory systems, HTM implementations can be extended to ensure that they become *crash-sync-safe*. Designing crash consistent HTM (ccHTM) requires augmenting HTM with a separate `undo/redo` log in persistent memory [9] and logging data modifications within a transaction. It is important to note that the software fallback path must also be made crash consistent through appropriate logging. In the event of a failure, the ccHTM logs can be used to restore the application’s persistent data to the most recent consistent state. While many different ccHTM implementations have been proposed recently [9]–[13], to the first order, they are all similar. In this work, we developed and implemented our own ccHTM design as a representation of the prior proposals.

**Transient caches.** For transient caches our ccHTM implementation augments a regular HTM [20] with support for failure-atomicity when modifying data in NVM. Apart from the usual read/write set tracking employed in HTM designs, ccHTMs employ a separate write-set log in NVM to maintain failure-atomicity. To update the NVM log, we

extend the hardware to issue write-combined, non-temporal stores (those that bypass the cache hierarchy, like x86’s `movnt` [21]) for every write within a transaction. These writes are non-transactional operations [22], so they do not become part of the transaction’s write set. Note that reads and writes that are part of the transaction use the regular temporal load/store instructions and are served from the CPU caches. We use `redo` logging in our `ccHTM` implementation, but `undo` logging would be similar. When used inside a hardware transaction, the `redo` log does not suffer from read indirection, because the values can be found as speculative values in the L1 cache. At commit time, we first ensure that the log writes are persistent, then atomically persist a log commit message in the NVM log, then make the transaction’s updates visible to other cores in the system. Overall, transactions first attempt an execution as a failure-atomic hardware transaction. However, if a hardware transaction aborts, the fallback path involves acquiring a global lock and executing pessimistically using a software `undo/redo` log. Next, we describe in detail the various aspects of our `ccHTM` implementation.

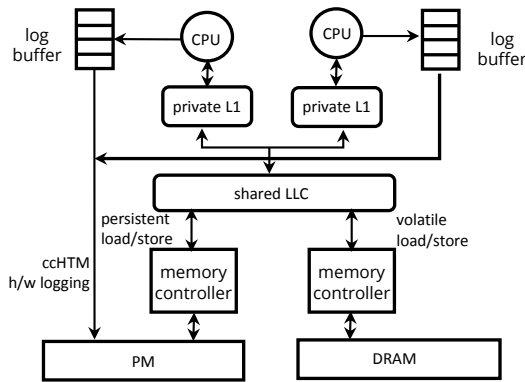


Fig. 1. Design of `ccHTM`

**Persistent write-set logging.** HTM runtimes keep track of the read/write sets of the executing transaction. Writes executing inside a transaction are held in the L1 cache in speculative state, isolated from the rest of the memory hierarchy until the successful completion and commit of the transaction. Similar to HTMs, `ccHTM` issues writes in the transaction to the L1 cache. In addition, `ccHTM` intercepts each write and augments it with a hardware based non-temporal log-write request into a thread-local NVM log. So, every write within a transaction results in a temporal write to the L1 cache and a non-temporal log write. The NVM log write is asynchronous to the transaction’s critical path. The `ccHTM` log is durable and atomic updates do not suffer from inherent read indirection overheads of logging, as incoming read requests are being served directly from the L1 cache.

**Transaction commit.** An `ccHTM` transaction comprises both volatile state (the cache lines held speculatively in the L1 cache) and persistent state (the `ccHTM`-log). Thus, the `ccHTM` transaction commit sequence differs from a traditional HTM commit. The `ccHTM` commit sequence includes: (1) updating the book-keeping structures of speculative cache-lines, (2) failure-atomic write-set log commit on NVM, and (3) atomically releasing the speculative cache-lines to the rest of the memory hierarchy. It is important to note that `ccHTM` commit operation combines two commit phases – a persistent memory commit, in the form of `ccHTM`-log commit, and a volatile memory commit, in the form of speculative cache-line unlocking. A

`ccHTM` log commit involves two `sfence` instructions. The initial `sfence` drains the buffered asynchronous log writes to the `ccHTM`-log. Next we atomically persist/update the `ccHTM`-log’s tail-index with the latest log-entry index value, followed by another `sfence`. The `ccHTM`-log’s tail-index update doubles as a commit-flag entry and enables fast log truncation. Once the transaction has been committed in NVM, the volatile commit is performed by atomically moving the affected cache-lines out of the speculative state. Once the volatile commit is performed, the transaction has successfully completed.

**Transaction abort.** Similar to HTM aborts, `ccHTM` aborts may be triggered due to (but not limited to) a load/store on another thread that conflicts with the current transactions’ write/read set, OS interactions like system calls or context switches, L1 cache capacity overflow. In addition to all of the HTM abort causes, `ccHTM` transactions abort if the runtime runs out of `ccHTM`-log space during hardware logging. We introduce a new abort flag called `NO_LOG_SPACE` to capture this abort cause. A transaction abort includes (1) discarding speculative L1 cache-lines, and (2) invalidating `ccHTM`-log appends. We rely on existing HTM capabilities to achieve (1). We do not explicitly invalidate `ccHTM`-log entries as they remain invalid till `ccHTM`-log’s tail-index update.

**Fallback path.** Similarly to hardware transactions, `ccHTM` transactions are best effort – the transactions are not guaranteed to complete. `ccHTM` transactions use regular write-ahead-logging (WAL) on the fallback path to ensure persistence. The fallback path transactions use either `undo` or `redo` logging while HTM transactions use `redo` logging. In addition, a global lock ensures the synchronization between the fallback path software transactions and `ccHTM` hardware transactions. To ensure isolation, the hardware transactions read the global lock as soon as they start executing, which makes them abort if another thread acquires the lock.

**Log truncation.** We truncate the transaction logs (both `ccHTM` and fallback path) at the end of each transaction – eager log truncation. With `redo` logging, log truncation involves first persisting the cache-lines modified as part of the transaction and then invalidating the transaction’s log entries. We truncate the `ccHTM` transaction logs as part of the transaction commit step, i.e., once the NVM log of the transaction is committed, we perform the following steps: (1) issue `clwb` requests to all the cache-lines in the write-set, (2) issue an `sfence` to ensure their writeback, (3) issue a non-temporal update request to atomically reset the `ccHTM`-log’s tail-index to truncate/invalidate all the previously written log entries, and (4) issue another `sfence` to ensure that the update request has been persisted. Once these four steps are performed, the volatile commit of the transaction is carried out. We also truncate the logs for the transactions executed in the fallback (software) path as soon as they commit. It is important to note that since both the fast path and slow fallback path employ log truncation, it is feasible to employ different logging techniques in the different paths. For example, it is possible to use `redo` logging in the fast path and `undo` logging on the fallback path. This design approach allows us to evaluate crash-consistency mechanisms that use different logging techniques on the different paths. Furthermore, this eager log truncation approach, relieves our `ccHTM` implementation of the burden of tracking the execution order of different transactions in their respective NVM logs, as is necessary in other prior approaches [11].

**Persistent caches.** In systems with persistent caches, speculatively updated `ccHTM` cachelines are persistent as soon as they are atomically released. (when they made visible in L1 cache). However, transactions executing in fallback path still need atomic updates in the

form of `undo/redo` logging. So, regular HTM implementations can be augmented with a fallback path log and can ensure crash-sync-safety with no additional changes to the HTM.

### B. Crash-sync-safe STM

Software Transactional Memory (STM) offers atomicity and isolated transactions for volatile memory. All the data modifications made within the transaction are made visible to other threads atomically when the transaction commits. If the transaction aborts, none of the data modifications made within the transaction become visible. STM implementations track the read and write sets of individual transactions to ensure transaction atomicity. Further more, they provide transaction isolation by detecting conflicting transactions that modify at least one common memory location and aborting some of them as necessary.

With persistent memory systems, STM implementations can be extended to ensure that they become crash-sync-safe, i.e., data modifications within a transaction will persist atomically and the dependencies are handled properly (§III). There are two broad approaches to designing crash consistent STM (ccSTM): (1) augment STM with a separate `undo/redo` log in persistent memory [4], [5] or (2) repurpose the write sets already maintained as part of the STM implementation to also function as a `undo/redo` log. In the event of a failure, the ccSTM logs can be used to restore the application’s persistent data to the most recent consistent state. In this work, we concentrate on ccSTM designs that maintain a separate `undo/redo` log, similarly to [4].

**Transient caches.** In systems with transient caches, in order to make sure their log entries are persistent (`undo` or `redo`), ccSTM designs have to write back the log entries from the processor caches to the memory controller. Furthermore, log entries have to be written back as per the ordering constraints of the logging mechanism employed (as discussed in § II-A) using carefully orchestrated `clwb`, `sfence`, and non-temporal store instructions (e.g., `movnt`).

**Persistent caches.** However, in systems with persistent caches, ccSTM log entries are persistent as soon as they are created (when they reach the L1 cache). So, regular STM implementations also ensure crash consistency with no additional changes in systems with persistent caches.

### C. Crash-sync-safe locking

This implementation of transactions acquires a global spinlock at the beginning of every transaction and releases it at the end of every transaction. While this naive implementation suffers from frequent false conflicts for multi-threaded applications, it does offer one advantage. It is a very light-weight approach when no concurrent transactions are executed by an application, an extreme case of which is a single-threaded application. Mostly, we use this design point for the sake of completeness in our `crash-sync-safety` design space analysis. While global locking achieves proper synchronization, to achieve `crash-sync-safety`, transactions are usually extended with either `undo` or `redo` logging, which we describe next.

**Transient caches.** In systems with transient caches, data can be considered persisted only once it has been written back from the volatile cache hierarchy to the memory controller using one of `clflush`, `clflushopt`, `clwb` instructions. Further more, some of these instructions are non-blocking, so applications need to issue a subsequent `sfence` to ensure that the instructions have been fully executed and the associated data is actually persistent.

`undo` logging systems have to ensure that log entries are persistent before they can allow actual memory locations to be modified within a transaction. As shown in Table I, `undo` logging systems use a combination of `clwb` and `sfence` instructions prior to every data update, i.e., every store instruction. This frequent use of blocking `sfence` instructions could result in severe performance degradation. `redo` logging systems have to ensure that all the redo log entries and the commit log entry are persisted by the end of a transaction. Further more, the commit log entry may persist only after all the redo log entries have been persisted. As shown in Table I, `redo` logging systems use a combination of `clwb` and `sfence` instructions within a transaction.

**Persistent caches.** However, in systems with persistent caches, data is considered persistent as soon it has been written to the L1 data cache. So, no writeback of data to the memory controller is necessary on such machines. On systems with persistent caches, `undo` logging implementations need to ensure that log entries are created before the data update, while `redo` logging implementations need to ensure that redo log entries are created for every update within the transaction and that the commit log entry is created before the completion of the transaction. Since x86 systems guarantee TSO, the program order of stores ensures that the stores belonging to the log entry creation and data update are performed in order, without the need for any intervening `sfence` or `clwb` instructions. For example, with persistent caches on an x86 machine, all the `clwb` and `sfence` instructions shown in Table I become obsolete. However, for systems with a weaker memory model (e.g., ARM), an appropriate `fence` instruction is necessary to ensure that the stores are executed in program order. Persistent caches significantly improve the performance of `undo/redo` logging systems as they eliminate expensive `clwb` and `sfence` instructions.

## V. IMPLEMENTATION AND EVALUATION METHODOLOGY

We want to understand the overheads of crash-consistency and crash-sync-safety, as well as what is the best implementation of a transactional library that provides these properties, given various NVM characteristics, persistence domains, and workload characteristics. To do so, we compare the performance of different transactional library implementations along the following axes: (1) Persistence domains of the system. Specifically, we consider systems with *persistent* and *transient* caches (§II-C). (2) Single-threaded vs multi-threaded applications. Single-threaded applications just require crash consistency while multi-threaded applications require crash-sync-safety (§III). (3) Evaluation platform – real hardware with Intel Optane DC NVM or an architectural simulator.

**Real Hardware vs Architectural Simulation.** To evaluate `ccHTM`, we use two different platforms: (1) bare-metal hardware with TSX and Intel Optane NVM and (2) SESC, a cycle-accurate simulator. While neither approach allows us to accurately evaluate `ccHTM`, they complement each other and provide a comprehensive analysis of the competing mechanisms. For example, simulation accurately models the proposed hardware changes not possible with TSX. However, real hardware more accurately factors in transaction abort rates introduced due to system jitter (background activities, thread context switches, cache capacity constraints) and the latency and bandwidth constraints of real NVM DIMMs.

**Intel Optane NVM hardware testbed:** We use a Intel Xeon server (Cascade Lake microarchitecture) with 96 cores over 2 NUMA sockets. We use Fedora Linux as the OS. The Intel processor supports restricted transactional memory (`rtm`) and the cache-line-write-back instruction (`clwb`). Each processor socket has access to 375 GB of

Processor	16 cores 1 GHz connected via bus-interconnect
L1 cache Ins & Data	64 KB per core / 64 B cacheline/ 8-way set associative
L2 cache Ins/Data	256 KB per core/ 64 B cacheline/ 8-way set associative/ hit-latency 18 cycles
L3 cache	16 MB shared/ 64 B cacheline/ 16-way/ hit-latency 34
Coherence protocol	MESI across L2 caches
NVM log size	10 MB per core/thread
NVM r/w latency	250/750 cycles

TABLE IV  
SIMULATOR CONFIG, ADOPTED FROM [24]

DRAM and 756 GB of Intel Optane NVM, configured in Direct Access Mode [23]. The NVM memory is managed by a DAX supporting file-system, hence applications have to explicitly map NVM memory into their process address space prior to using the NVM. Therefore, we modify our applications to explicitly allocate all memory dynamically from the NVM address space using the `libvmem` allocator from the Persistent Memory Development Kit (PMDK) [14]. We allocate persistent memory (`mmap`) from the closest NVM DIMM (NUMA aware). We bind each of the application threads to a compute core. Thread binding prioritizes the compute cores within the same NUMA socket and assigns compute cores from a different socket only when an application uses up all the cores in the current socket. Out of five runs, we report the mean of the middle three runs.

**Simulator:** We implemented `ccHTM` as an extension to `SESC-HTML` [24], which emulates the instruction behavior (commit, abort, etc.) within the `HTM_begin()` and `HTM_end()` code regions and passes them to a back-end timing module for simulation. We augment the writes happening within a HTM transaction with an asynchronous, non-temporal log-write to the NVM resident log, in addition to the temporal L1 cache write. Furthermore we implement the `clwb` and `sfence` instructions necessary for the correct functioning of software-based crash-consistency mechanisms. Table IV lists the configuration of the various hardware structures modeled in our simulator. Since `SESC` was designed for MIPS, we cross compile the `STAMP` benchmarks and the `ccHTM` library into a MIPS binary. **Workloads.** We use two benchmarks from the PMDK project [14], namely C-tree and Hashmap. These two benchmarks implement a persistent crit-bit tree and a hashmap. We port these two applications to use different persistent memory transactional mechanisms. We run the `pmembench` workload generator provided with PMDK and use workload parameters from [6]. In addition, we use the transactional applications from `STAMP` [25], a popular benchmark suite used by others to evaluate libraries for NVM [6], [26], [27]. We augment transactions with crash-consistency, on top of the atomicity, consistency, and isolation guarantees already provided. To better understand these workloads, we instrumented the simulator to count the load/stores for each transaction.

## VI. EVALUATING CRASH-SYNC-SAFETY

In this section, we seek to understand the cost of implementing crash-sync-safety (§III) in various ways. To do so, we evaluate multi-threaded applications that provide both `crash-consistency` and `synchronization`. We use the crash-consistency mechanisms in Table III. We use a spinlock to ensure correct synchronization for the `undo/redo` logs and on the fallback path of the HTM. We want to answer the following questions: (1) What is the most efficient implementation of crash-sync-safe transactions? To answer

this question, we compare HTM-based crash-sync-safe transactions with STM-based crash-sync-safe transactions and with `undo/redo` logging using a spinlock. (2) What is the overhead of achieving crash-sync-safety? To answer this question, we compare to a sequential implementation baseline, with no `crash-consistency` and no `synchronization`. (3) What is the overhead of crash-consistency for multi-threaded applications that are properly synchronized? To answer this question, we compare with a non-crash-consistent baseline (HTM+spinlock). (4) How does the persistence domain of the NVM influence the results? To answer this question, we consider two different NVM devices: one with transient caches (§VI-A) and one with persistent caches (§VI-B). Current HTM for systems with transient caches ensure proper `synchronization`, but not `crash-consistency`, so our real hardware evaluation on transient caches only approximates a crash-sync-safe implementation based on HTM. Therefore, we use simulation to properly evaluate the overheads of the crash-sync-safe HTM.

**Summary of crash-sync-safety results.** We evaluate multiple transactional implementations on real hardware with the new NVM devices, as well as using an architectural simulator. Our results are summarized below. (1) We find that `ccHTM` consistently outperforms other transactional implementations, by 0.06X-30X (at 8 threads) for transient caches, and by 3X on average for persistent caches. The only exceptions are applications which are known for being problematic for hardware transactions, i.e., with large read or write sets that overflow the cache, or with unsupported instructions that always abort the hardware transactions. Therefore, extending HTM with `crash-consistency` for transient caches is the most promising solution to provide crash-sync-safe transactions. The simulation results show that making the HTM crash-consistent does not add significant overhead compared to a non-crash-consistent HTM (HTM+spinlock). For persistent caches, current HTMs (e.g., TSX) are already crash-sync-safe. (2) When using `ccHTM` to achieve crash-sync-safety, it comes almost for free. The overheads of crash-consistency are subsumed by synchronization overheads and, as applications scale, performance increases compared to single-thread execution. When the `ccHTM` implementation does not achieve scalability due to aborts, the `ccSTM` still ensures this property. (3) If we disregard scalability improvements given by running multiple threads, we can measure the cost of crash-consistency compared to a non-crash-consistent solution that still ensures the synchronization. On average, HTM+undo(redo) is 2.3X (2.4X) slower than HTM+spinlock (for 4 threads), for transient caches. When caches are persistent, this cost becomes negligible. (4) In multi-threaded applications, the persistence domain still plays a very important role, but the results are not as dependent on it as they are for the single-threaded applications. The overhead of crash-consistency is considerably lower when caches are persistent. In addition, HTM is `crash-consistency` out of the box, so no changes are necessary.

### A. Transient CPU caches

We use our real test-bed and architectural simulator to evaluate the cost of crash-sync for transient caches.

**Real.** Figure 2 shows the scalability of the various approaches outlined above with varying number of threads, on real hardware, using Intel TSX for the HTM. HTM+undo (HTM+redo) outperforms `undo (redo)` for vacation, `kmeans`, `ssca2`, `intruder` and `genome` by 3.6× (3.7×), 30.8× (18.3×), 13.3× (7.1×), 0.6× (0.6×) and 4.9× (4.8×), respectively, at 4 threads. The only exception is `labyrinth`, where many transactions overflow the cache and abort, ending up executing on the fallback path (`undo/redo`), serialized by a spinlock.

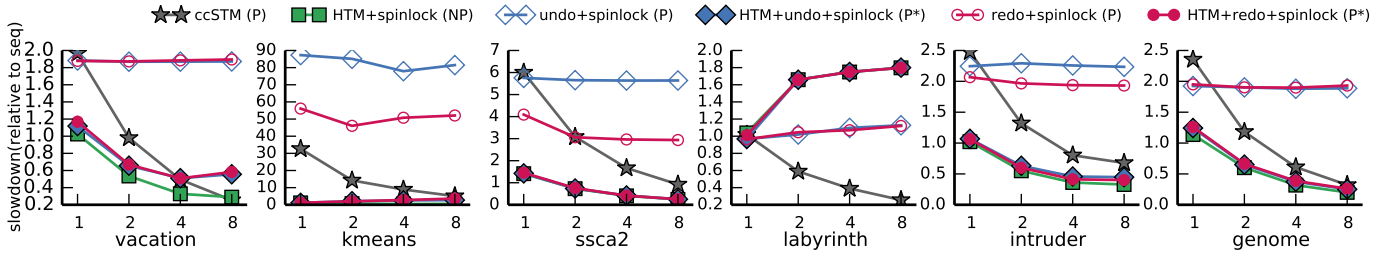


Fig. 2. TSX-enabled hardware with real NVM and transient caches by number of threads (X axis). (P) crash-consistent; (NP) not crash-consistent; (P\*) approximates crash-consistent solution.

Compared to the `ccSTM`, `HTM+undo` (`HTM+redo`) is faster for `vacation`, `kmeans`, `ssa2`, `intruder` and `genome` by  $1\times$  ( $1\times$ ),  $3.5\times$  ( $3.2\times$ ),  $3.9\times$  ( $4.0\times$ ),  $1.7\times$  ( $1.9\times$ ) and  $1.6\times$  ( $1.5\times$ ) respectively and slower on `labyrinth` by 53.06% (53.10%) at 4 threads. Choosing between software and hardware transactions largely depends on the workload, especially the size of the transactions, conflict rate and usage of TSX-unsupported operations. `ccSTM` performs better on workloads with larger transactions (e.g., `labyrinth`) or more contention and scales better to a larger number of threads. We attribute this behavior to its better conflict resolution. However, for small transactions, the software conflict detection and resolution of the `ccSTM` introduces too much overhead, which is greatly reduced by the simpler hardware-based requester-wins policy of the `HTM`.

We approximate the cost of `crash-consistency` for multi-threaded applications by comparing to `HTM+spinlock`, which suffers from the overheads of synchronization, but not `crash-consistency`. `HTM+undo` and `HTM+redo` are, on average,  $2.3\times$  and  $2.4\times$  slower than `HTM+spinlock` for all workloads (at 4 threads).

As in the single-thread applications, the choice between `undo` and `redo` logs greatly depends on the workload characteristics. However, when we use `HTM` on the fast path, the differences between `undo` and `redo` logs on the fallback path are significantly diminished with `HTM+undo` and `HTM+redo` resulting in similar performance.

We compare the `ccSTM` with an `STM` to understand the cost of `crash-consistency` for the `STM`. `ccSTM` is at most  $8.2\times$  slower than an `STM` with no `crash-consistency` for 1 thread and at most  $7\times$  slower for 8 threads. We see that while `crash-consistency` definitely adds a noticeable overhead, it does not impact the scalability of the original `STM`. Moreover, the difference between `ccSTM` and `STM` decreases with increasing the number of threads, showing that the overhead of fences is amortized between multiple concurrent threads.

Finally, the cost of `crash-consistency` does not tell the entire story, as we provide both `crash-consistency` and `synchronization` for multi-threaded applications. Thus, we also measure the cost of `crash-sync-safety` by comparing with a baseline with no `crash-consistency` and no `synchronization` (`seq`). While `crash-consistency` adds overhead compared to volatile in-memory execution, efficient `synchronization` often improves performance by enabling the application to scale to multiple threads. Therefore, the cost of `crash-sync-safety` is much lower than the cost of `crash-consistency` when we can pair efficiently `synchronization` and `crash-consistency`, using `STM` or `HTM`. However, when we use distinct methods for the two, the overheads compose and the cost of `crash-sync` is much higher, as exemplified by `undo/redo` using spinlocks being  $.9\times/1.4\times$  and  $2.7\times/2.9\times$  expensive than `ccHTM+undo/redo` and `ccSTM` on-

average.

As in §VII-A, these numbers are an approximation of `ccHTM` results, as only the fallback path is crash-consistent. We evaluate a full-fledged `ccHTM` in the simulator in the next section.

**Simulated.** Figure 3 shows `ccHTM` results using simulation. We use this to confirm that adding `crash-consistency` on the `HTM` fast path does not hinder its performance. Once again, the general trends from real hardware largely hold in the simulated environment as well: (1) `HTM+undo/HTM+redo` comfortably outperform `undo/redo`. For example, for `Vacation` benchmark with 4 threads, the improvements are  $3\times$  and  $6\times$  respectively. The only exception to these general trends are seen in the case `Labyrinth`, where `undo` and `redo` perform better than `HTM` based approaches due to the high transaction abort rates inherent to the workload. (2) `undo/redo` exhibit the highest overheads and poor scalability due to the spinlock. (3) All `crash-consistency` mechanisms increase execution time over the non-crash consistent baseline, `HTM+spinlock`. However, on-average `ccHTM+spinlock` increases execution time by only 8% compared to `HTM+spinlock`. The simulation results differ from the real hardware results mainly in the scalability showed by `ccHTM`. This difference comes from the system events that occur in the real systems, but are hard to model in a simulation environment.

### B. Persistent CPU caches

We use our bare-metal test-bed to emulate persistent caches. `TSX` ensures `crash-sync-safe`. We show the results in Figure 4. As expected, `undo` and `redo` perform the worst and exhibit poor scalability because they serialize all transactions using a global spinlock. `HTM+undo` (`HTM+redo`) is  $2.4\times$  ( $2.4\times$ ) faster than `undo` (`redo`) on average for all workloads at 4 threads. The only exception is `labyrinth`, which causes frequent transaction aborts due to overflows. While `STM` incurs high overheads in low contention scenarios (1 or 2 threads) or when transactions are small, it exhibits good scalability due to its fine-grained locking and generally performs the best at 8 threads and for large transactions. `STM` is  $1.6\times$  ( $2.0\times$ ),  $6.9\times$  ( $6.9\times$ ) faster than `HTM+undo` (`HTM+redo`) for `vacation` and `labyrinth` at 8 threads.

## VII. EVALUATING CRASH-CONSISTENCY

In this section, we seek to understand what is the cost of `crash-consistency` for single-thread applications, i.e., when applications do not require `synchronization`. To do so, we perform an exhaustive study using multiple hardware platforms, using simulation and emulation when the actual hardware is not available. We evaluate both transient (§VII-A) and persistent caches (§VII-B). We present the results relative to a sequential execution baseline (`seq`) that does not provide `crash-consistency` nor `synchronization`. We evaluate the `crash-consistency` mechanisms described in Table III.

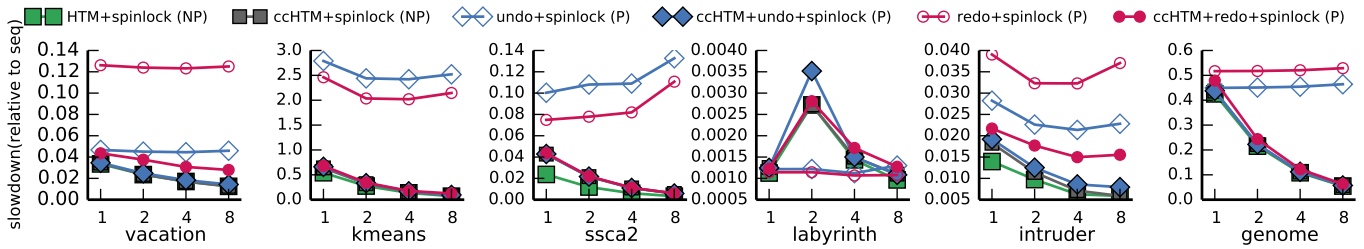


Fig. 3. Simulation, transient caches by number of threads (X axis). (P) crash-consistent; (NP) not crash-consistent; (P\*) approximates crash-consistent solution.

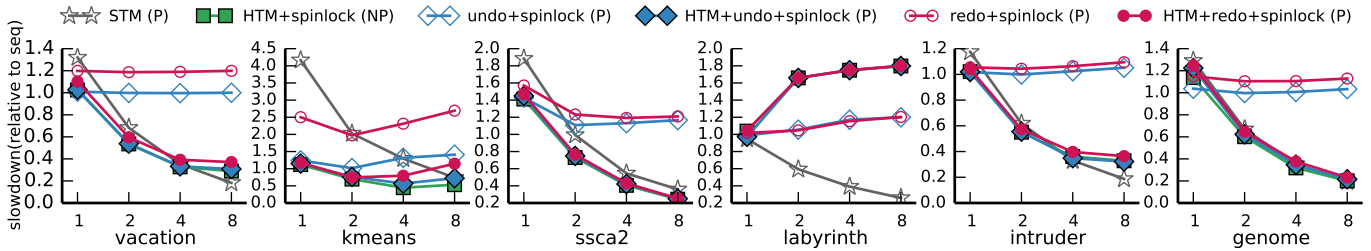


Fig. 4. TSX-enabled hardware with real NVM and emulated persistent caches by number of threads (X axis). (P) crash-consistent (NP) not crash-consistent.

The goal of this evaluation is to understand the cost of `crash-sync-safety` relative to only providing `crash-consistency`, and whether providing `crash-sync-safety` provides any benefits from a performance perspective compared to simply providing `crash-consistency`. We see that `crash-sync-safety` is a useful implementation property, as it can lower the cost of `crash-consistency` by scaling applications to multiple threads. For example, in the `vacation` benchmark achieving `crash-sync-safety` for 8 threads improves performance by  $0.7\times$  compared to non-crash consistent single-thread execution, despite the `crash-sync-safety` property due to `ccSTMs` scalability. In contrast, the `undo` log causes a slowdown of  $0.85\times$  to achieve crash consistency only (for a single-thread execution). In this section, we breakdown the costs of crash-consistency and characterize single-thread applications.

**Summary of crash-consistency results.** We find that the persistence domain plays a crucial role in choosing the best `crash-consistency` method. The same mechanisms have very different behavior and performance characteristics on systems with transient caches versus systems with persistent caches. In particular, `HTM` is an interesting case-study. For systems with persistent caches, `HTM` guarantees `crash-consistency` out of the box, with no architectural changes, while for transient caches, `HTM` needs architectural changes to ensure `crash-consistency`. In both cases, `HTM` also provides correct synchronization, and incurs the associated costs, although all applications we consider in this section are single-threaded and do not require synchronization.

From our empirical results, we can draw the following conclusions: (1a) In systems with transient caches, `HTM` benefits `crash-consistency`, despite its synchronization costs and required architectural changes. The reason for this is that `HTM` based `crash-consistency` systems are able to reduce the number of expensive cache line flush and fence instructions used in pure software `undo/redo` logging techniques. (1b) The choice between `undo` and `redo` logging vastly depends on the appli-

cation characteristics and the size of the read and write sets of the transactions. (2a) In systems with persistent caches, the `HTM` benefit for `crash-consistency` is reduced, as software logging mechanisms do not require expensive flush and fence instructions anymore. In this case, the `HTM`'s synchronization overheads become apparent. (2b) `undo` logging is the best choice for ensuring `crash-consistency` when caches are persistent, since `redo` logs still suffer from read-indirection overheads.

Overall, persistent caches provide a significant advantage, as the overhead of `crash-consistency` on average over `seq` is only 1% for the best method (`undo`), compared to 6% for best method when caches are transient (`HTM+redo`).

#### A. Transient CPU caches

We compare the performance of the various crash-consistency mechanisms on systems with transient CPU caches (§II-C), on both real hardware and our architectural simulator (§V).

**Real.** In this experiment, we evaluate all crash-consistency mechanisms on the real hardware using a server with support for TSX and we show the results in Figure 5. As expected, all crash-consistency mechanisms increase execution time compared to a non-crash-consistent baseline (`seq`). However, `HTM+undo` and `HTM+redo` significantly outperform their pure software counterparts (`undo` and `redo`), improving performance by as much as  $98\times$  and  $97\times$ , respectively. This is due to the `HTM` reducing the number of fences and read-indirection for the transactions that succeed. The only exception is `Labyrinth`, where `HTM+undo` and `HTM+redo` perform similar to their software counterpart, due to more frequent aborts caused by large transaction sizes (`Labyrinth`). These results indicate the best performance that we can expect from a `ccHTM` on real hardware, as we approximate the performance using `HTM+undo/redo` that only provides `crash-consistency` on the fallback path, but not inside the hardware transaction. Therefore, these results measure the upper limit of `ccHTM` performance, we also evaluate it in the simulator (Fig. 6).



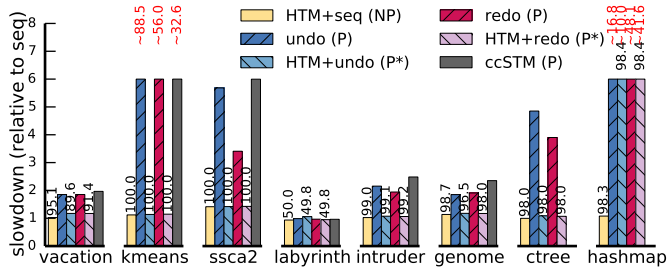


Fig. 5. TSX-enabled hardware, with real NVM and transient caches. We show transaction success rate for methods using HTM (values in black). We truncate large bars in Kmeans and hashmap (values in red). (P) crash-consistent; (P\*) approximates a crash-consistent solution; (NP) not crash-consistent.

The transaction success rate<sup>1</sup> varies from from 49% (Labyrinth) to 100% (Kmeans) - also shown in Figure 5.

HTM+undo and HTM+redo are on average 14% and 12%, respectively, of the ideal baseline, seq, showing that crash-consistency can be ensured at a small performance penalty using HTM. Although not needed for single-threaded applications, HTM also provides synchronization. To understand this additional overhead, we also evaluated HTM+seq, which ensures synchronization when transactions succeed, but not on the fallback path. HTM+seq, incurs overheads, ranging from 2.5% (intruder) to 13% (genome), even when no crash consistency guarantees are provided. These overheads are due to hardware book-keeping to execute transactions and transaction aborts.

All pure software crash-consistency mechanisms (undo, redo and ccSTM) greatly increase execution times – as much as 41 $\times$ , 89 $\times$  and 33 $\times$  respectively (for Kmeans). redo logging generally performs better or as well as undo logging for the workloads evaluated, but the results highly depend on the number of reads and writes in the transaction. undo suffers the overhead of flushing and fences for every write, while redo suffers the overhead of read indirection, proportional to the number of reads and the size of the log. ccSTM incurs the highest overhead across all workloads. We attribute this to the higher synchronization overheads of the ccSTM, in addition to the software logging overheads like undo and redo.

**Simulated.** In this experiment, we use the simulator to evaluate ccHTM for transient caches with the proper architectural changes. Figure 6 shows the results. The trends from the real hardware still largely hold here. ccHTM-undo and ccHTM-redo have lower overheads than their software counterparts by as much as 3.2 $\times$  and 2.7 $\times$  (Kmeans) respectively. And they both come within 1.2 $\times$  of the ideal baseline, seq. Even with full support for crash-consistency, ccHTM outperforms other methods. The only exception is Labyrinth, where ccHTM suffers comparable overheads to its software counterparts due to frequent transaction aborts. However, the transaction abort rate is less in the simulator than on real hardware as the simulator models overflow and some unsupported instructions, but not all events that would cause a transaction to abort on real hardware. We attribute these differences to inaccuracies between the hardware implementation details within the simulator and proprietary commercial hardware. ccHTM-seq adds 28.62% overhead on average for all benchmarks compared to seq, highlighting that the architectural changes made to the HTM have fairly low impact.

<sup>1</sup>TSX transactions are best-effort, so they might abort even for single-thread workloads, when there are no conflicts.

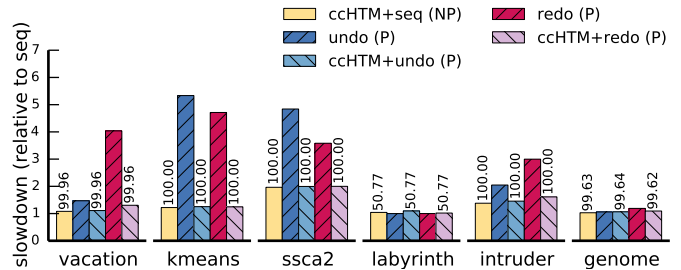


Fig. 6. Simulation, transient caches. We show transaction success rate on top of the methods using HTM. For each method, we specify if it is crash-consistent (P) or not (NP).

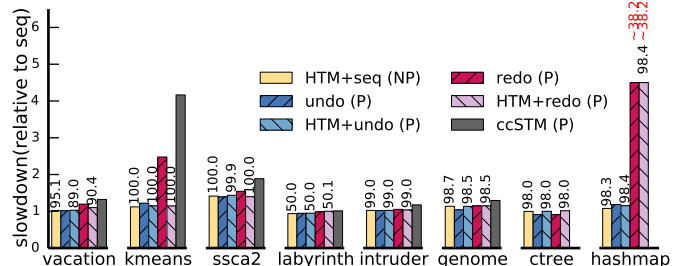


Fig. 7. TSX-enabled hardware with real NVM, emulating persistent caches. We show transaction success for methods using HTM (values in black). We truncate large bars in hashmap (values in red). (P) crash-consistent; (NP) not crash-consistent.

### B. Persistent CPU caches

In this experiment, we use our bare-metal testbed (§V) to emulate persistent caches (§II-C). We show the results in Figure 7. Unlike for transient caches, here HTM+undo and HTM+redo perform worse than undo and redo by at most 10%. When caches are persistent, undo and redo logging techniques no longer have to use expensive cache line flush and fence instructions to ensure data consistency, while the HTM still has the overhead of ensuring synchronization. To quantify the overhead of the HTM, we measure HTM+seq, which is up to 40% slower than seq, while undo and redo are up to 40% and 37 $\times$  slower. The STM has even higher synchronization overhead on average, being up to 3.1 $\times$  slower than seq. Moreover, undo and redo perform similarly in most cases, except in the case of hashmap and Kmeans, where undo performs better than redo. Although both methods are faster because they don't require fences and flushes, redo still has the overhead of read indirection in certain workloads with many reads and writes. Moreover, an application can be tuned to use one technique or the other, which we show with hashmap as an example. Hashmap is tuned to use undo logging with PMDK library and thus perform better with undo logging.

## VIII. RELATED WORK

Mnemosyne [4] and NV-Heaps[5] were the first to extend an STM for providing persistence when caches are transient. Recent research [28], [29] further improves the scalability of durable STMs with better concurrency-control protocols, DRAM+NVM hybrid logging-schemes, etc. The ccSTM that we evaluate closely follows the design proposed by Mnemosyne, but the insights are equally applicable to other durable STM proposals. Atlas [30] extends critical sections based on locks with persistence semantics and guarantees failure-atomicity of outer-most critical sections. NVThreads [31] builds on

Atlas to provide a drop-in replacement for pthreads that enables NVM crash-consistency. SFR [32] on the other hand, provides persistence at thread regions delimited by synchronization operations. Atlas [30], SFR [32] and other proposals [33], [34] essentially use data-race-free (DRF) property of correctly synchronized programs and support compiler/ISA level fast-persistence with NVM. Therefore, our lock based redo/undo log evaluations broadly model the performance characteristics of these proposals.

DudeTM [35] extends an HTM for persistence using a shadow copy of the NVM data in volatile memory. Unlike DudeTM, ccHTM does not incur the overhead of additional shadow copies. PHTM [9] extends a persistent HTM using non transactional stores and transparent flush semantics to ensure crash-consistency. PHTM was extended in PHyTM [10] by adding an STM in the fallback path. Both PHTM and PHyTM emulate logging inside the HTM region using regular load/stores instead of their non transactional stores and transparent flush support. Thus, their design affects the read/write set and capacity aborts. In addition, PHTM and PHyTM provide only an approximation of their system performance using a TSX host, but no implementation of their proposed hardware extensions. NV-HTM [36] introduces HTM accelerated persistent memory transactions without changing the existing HTM hardware protocols. NV-HTM differs durable log-commit till HTM-end for correctness reasons, and thus misses out on overlapped durable log-writes(ccHTM).

Intel added new instructions `clflushopt` and `clwb` for efficient transient cache-line flush [21]. Researchers have proposed persistency models [6], [37]–[40] to reason about crash-consistency for NVM. Various proposal to perform efficient logging and paging for NVMs are also proposed [41]–[46]. Additionally, there has been increasing interest in developing persistent transactional memories or memory architectures for NVMs with transient caches [9], [11]–[13], [26], [27], [47]–[50]. Moreover, various applications have been ported to use NVM and have been shown to increase performance [51], [52].

Persistent caches [44], [53], [54] may become prevalent. Recent work uses logging with persistent caches to provide durability guarantees [55], [56]. Our work studies tradeoffs of providing crash-sync-safe for both persistent and transient caches.

## IX. CONCLUSION

In this paper, we provide an extensive study of NVM crash-consistency mechanisms for persistent and transient caches. Our findings indicate that the persistence domain determines the cost of crash-consistency, but we can reduce the overhead by scaling-up to multiple threads and combining crash-consistency with synchronization.

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